Corner Protection To Reduce Wrap Around

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ABSTRACT OF THE DISCLOSURE

A method and structure are provided with reduced gate wrap around to advantageously control for threshold voltage and increase stability in semiconductor devices. A spacer is provided aligned to field dielectric layers to protect the dielectric layers during subsequent etch processes. The spacer is then removed prior to subsequently forming a part of a gate oxide layer and a gate conductor layer. Advantageously, the spacer protects the corner area o the field dielectric and also allows for enhanced thickness of the gate oxide near the corners.